

A single chip FPGA-based cross-coupling multi-motor drive system

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Abstract: Often, the demand for optimal and harmonious operation of multi-motor control systems requires sharing of feedback information from one drive to other drives. From the point of view of controller implementation, a multi-controller structure degrades the system integration and requires data communication among chips. The aim of this paper is to propose a fully integrated single chip solution for a cross-coupling multi-motor control system. The proposed speed controller with time-division multiplexing scheme can simplify the entire system, making possible the implementation on a single device. The experimental results confirm the implementation feasibility and the effectiveness of the proposed single chip system.

Keywords: cross-coupling, FPGA, multi-motor, PMSM, time-division multiplexing

Classification: Electronic instrumentation and control

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1 Introduction

There are several application domains that require more than one electric motor to be controlled and executed simultaneously in the same system, such as paper and textile manufacturing, automobile, and steel industry. Some of these industries require a motor drive system that can smoothly synchronize a group of multiple motors during the production process. The poor speed synchronization of multi-motor systems may cause varying catastrophic effects from the loss of dimensional accuracy to unstable processes and production reliability. In steel industry, rolling mill process is the operation where metal strips are successively passed through a number of rolling pairs to reduce the steel thickness [1]. In order to achieve the uniform metal stripe without irregular deformation, it is essential to smoothly synchronize a group of multiple motors at the same speed [2].

Nowadays, FPGA technology has been recognized as a promising candidate and widely adopted for the controller platform in embedded control systems [3, 4, 5], including high performance AC motor drives [6, 7, 8]. For multi-motor control systems, the demand of numerous resources and embedded multipliers for control algorithms often limits the number of controlled motors within a single chip. In literature, some previous works have successfully demonstrated, such as X-Y table system [9, 10], two-wheel driven electric vehicle [11, 12, 13]. By considering a multi-motor system containing several motor units, a massive number of FPGA resources and embedded multipliers are required for hardware realization, which leads to design constraints for a single chip FPGA device.

2 System description of the proposed single chip solution

In this paper, a single chip FPGA-based solution for multi-motor control system applicable for rolling mill drives is demonstrated. A cross-coupling controller for speed synchronization is presented, aiming to minimize the speed synchronization error caused by motor torque variation during the production process. To minimize resource requirements for such control algorithms, an area-efficient resource shar-

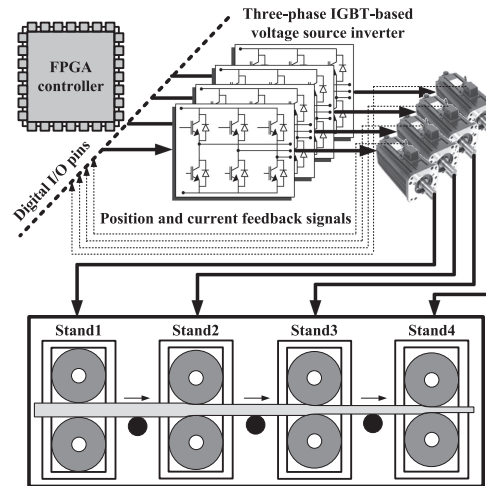


Fig. 1. Structure of a single chip FPGA-based controller for four rolling mill drives.

ing based on time-division multiplexing approach is introduced. The entire system is developed on a four-unit permanent magnet synchronous motor (PMSM) drive system with space vector pulse width modulation (SVPWM) based vector control scheme. Fig. 1 shows structure of a single chip FPGA-based controller for four rolling mill drives.

2.1 Cross-coupling control for speed synchronization

In this paper, the synchronization control strategy is based on the concept of relative-coupling control introduced in [14], with modifications in term of control architecture and implementation. The proposed multi-motor control system is implemented with the relative-coupling method for a four-unit PMSM motor drive system, as shown in Fig. 2, and is referred to as “cross-coupling control” whereas an independent control multi-motor system is referred to as “conventional control” throughout this paper. The main idea of relative coupling control is to subtract the feedback speed of each motor from other remaining motors, and the sum of speed differences is used as a compensation signal to the speed control loop. In this way, the speed variation on one motor caused by load disturbances can be compensated

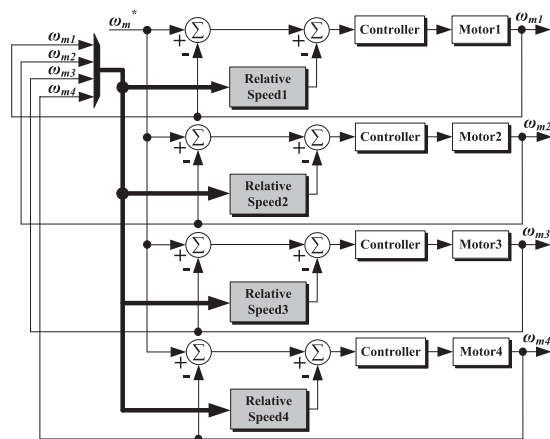


Fig. 2. Block diagram of the relative-coupling control structure for a four-unit motor drive system.

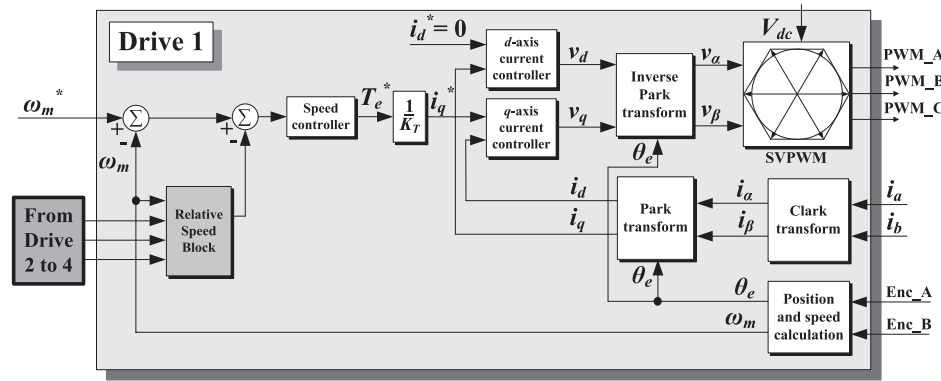


Fig. 3. Internal structure of a SVPWM-based vector control scheme with relative-coupling control for one rolling mill drive.

simultaneously. The speed response of all motors in the system can be equally maintained during the transient operation. The internal structure of a SVPWM-based vector control scheme with relative-coupling control for one drive system is shown in Fig. 3.

2.2 Area-efficient time-division multiplexing scheme

The concept of time-division multiplexing is to switch several input streams into a series of time slots, and transfer processing data across a single hardware module. Fig. 4 shows a simplified block diagram of the hardware architecture with the time-division multiplexing scheme. The operational steps can be described as follows: (1) A count-limited counter running with a clock rate of 50 MHz (a sampling time $T_s = 2 \times 10^{-8}$ s) is used to generate a common control signal to the multiplexer unit for selecting one of four-unit motors; (2) The multiplexer unit is executed simultaneously for transferring control parameters into a single hardware module; (3) The SVPWM-based vector control algorithm is executed continuously within different time segments, beginning from the first motor to the fourth motor; (4) The steps (1) to (3) are repeated sequentially for all computational operations starting from the Clark's and Park's transformation module, the speed and current PI regulator modules, the inverse Park's transformation module, and the SVPWM generator module. (5) After finishing the execution of the entire control algorithm, the controller module generates three sets of PWM output waveforms; (6) The demultiplexer unit separates each of the generated PWM output waveforms into four separate channels for controlling four sets of controlled machines.

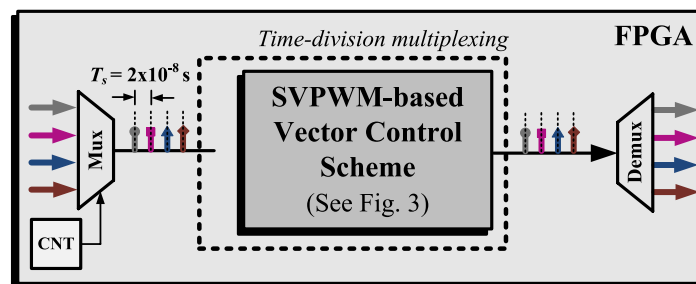


Fig. 4. Block diagram of the hardware architecture with the time-division multiplexing scheme.

2.3 Hardware solution using analog multiplexers

Since the number of motor units that can be controlled is also physically limited by the I/O interface pins on a FPGA, a hardware solution using analog multiplexers is presented in order to reduce the required I/O pins and the ADCs. In this paper, an analog multiplexer is employed to measure the motor current of four motors as shown in Fig. 5. With this approach, the same phase current of four motors can be managed by using only a single I/O pin with a common ADC. Since the motor windings are arranged with star connection, measuring of only two phase currents is sufficient enough by using only two analog multiplexers and two ADCs. The same connection diagram can be applied for measuring another phase current.

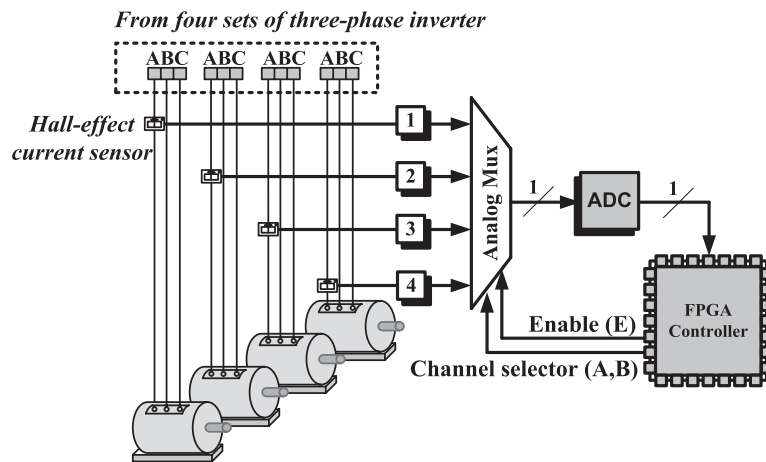


Fig. 5. Connection diagram of the hardware solution using an analog multiplexer (example showing measuring only current phase-A).

3 System development and experimental setup

The complete hardware module has been designed and fully integrated on a Xilinx XC3S1600E FPGA. The entire control system consists of a motor controller module, a multiplexing and demultiplexing module, and other auxiliary modules, including the ADC and DAC interface, serial communication for real-time GUI interface, and a fault protection module. The motor controller consists of position and speed calculation module, rotating coordinate transformation module, speed and current PI regulator module, and the three-phase SVPWM generator module.

For experimental setup, the motor specifications and parameters for the four identical low-power PMSM motors (PMSM1 to PMSM4) are summarized in Appendix. The scale-down laboratory system consists of PMSM motors, three-phase IGBT-based inverters, a Spartan-3E 1600E development board, 12-bit ADCs and DACs, analog multiplexers and dead time generator circuits. The common voltage of DC bus is set to 36 V and the switching frequency of PWM inverter is set to 16 kHz. The motor optical encoder has a resolution of 2,500 ppr (pulses per revolution). Fig. 6 shows a connection diagram of FPGA pin interface for implementing four-unit PMSM motor drive system.

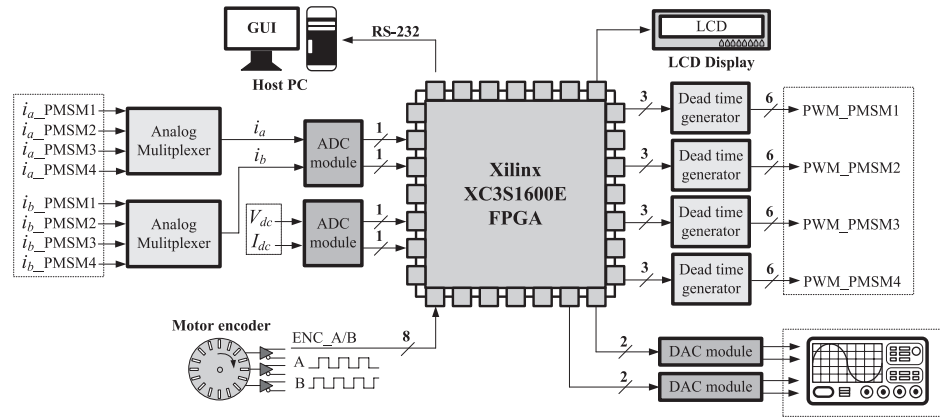


Fig. 6. Connection diagram of the FPGA pin interface for implementing the four-unit PMSM motor drive system.

4 Experimental validations

Initially, an experimental system has been set up to demonstrate the implementation feasibility of the proposed single chip solution with the time-division multiplexing scheme. Fig. 7 shows dynamic speed responses of the four PMSM motors during a speed-step command applied to PMSM1. Fig. 8 shows experimental results of the three-phase PWM waveforms (filtered), vector sector, and electrical position when PMSM1 is running at 1200 rpm. The experimental results prove that the proposed system with a time-division multiplexing scheme can operate a group of four motors independently. The external disturbance applied to one motor has no influence on other motors.

In order to evaluate the control performance of the proposed single chip system with a cross-coupling control scheme, a comparative study between a conventional independent control and a cross-coupling control scheme has been performed. Fig. 9 and Fig. 10 show a comparison of dynamic speed responses and speed synchronization error between a conventional control scheme and a cross-coupling control scheme, respectively, for four-unit motor drive system. The experimental results confirm that a single chip cross-coupling drive system with time-division multiplexing scheme can provide good disturbance rejection with less speed synchronization error compared to a conventional control scheme.

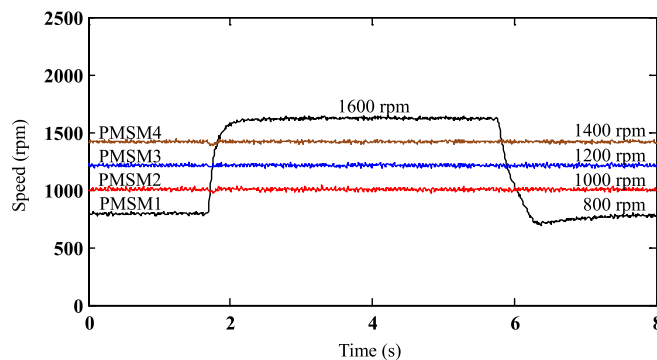


Fig. 7. Experimental results showing the dynamic speed responses of the four motors during a speed-step command applied to PMSM1.

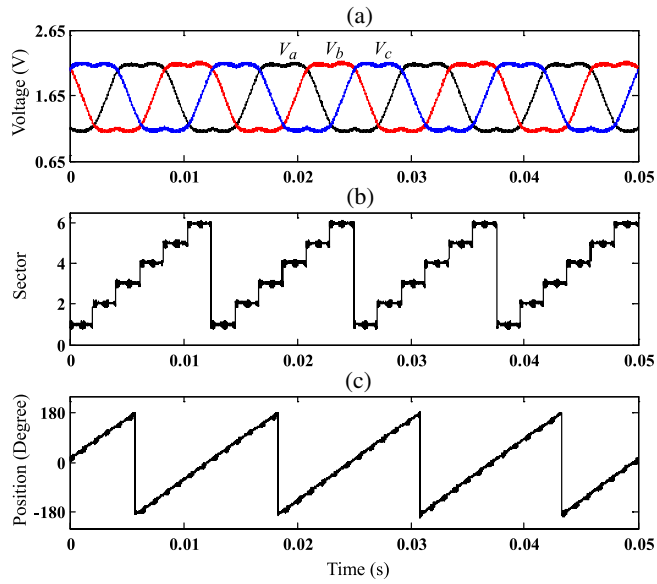


Fig. 8. Experimental results showing: (a) Three-phase filtered PWM waveforms; (b) Vector sector; (c) Electrical position when PMSM1 is running at 1200 rpm.

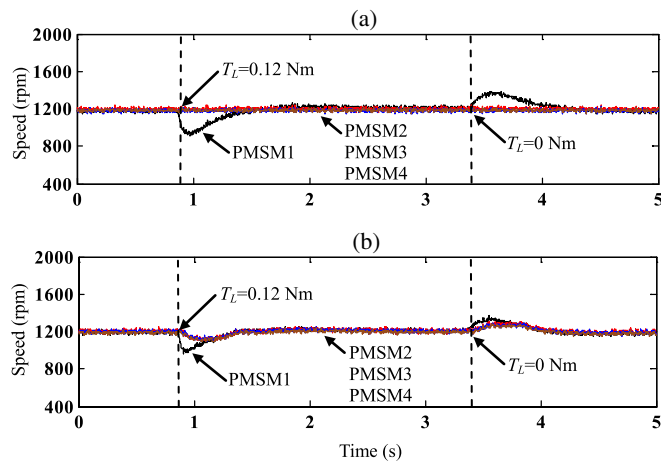


Fig. 9. Experimental results showing dynamic speed responses during load disturbances applied to PMSM1: (a) Conventional control; (b) Cross-coupling control.

For the latency analysis of a single-motor system, the current acquisition using the ADCs requires 204 clock cycles, the computational blocks for motor controller (Clark and Park transformations, current and speed PI controllers) take 38 clock cycles, and the SVPWM module needs 58 clock cycles. Thus, the whole algorithm execution requires a total of 300 clock cycles, meaning $6 \mu\text{s}$ at 50 MHz clock rate. For a four-motor system, the time-division multiplexing scheme introduces more computational time for running different control algorithms sequentially on the same hardware structure. In this paper, the proposed four-motor system with time-division multiplexing takes a total computation time of $7.08 \mu\text{s}$ ($37.1 \mu\text{s}$ when implemented with analog multiplexers), which is much less than the sampling interval of the inverter, $62.5 \mu\text{s}$ (16 kHz), and hence does not affect the control performance of the overall system. Fig. 11 shows a comparison of speed response between a single-

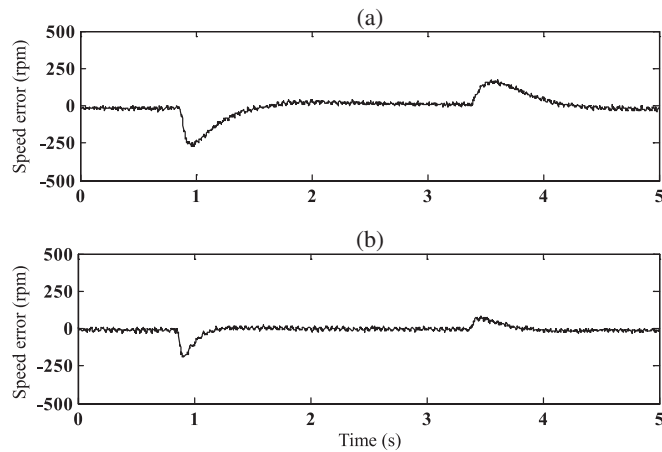


Fig. 10. Experimental results showing speed synchronization error between PMSM1 and PMSM2: (a) Conventional control; (b) Cross-coupling control.

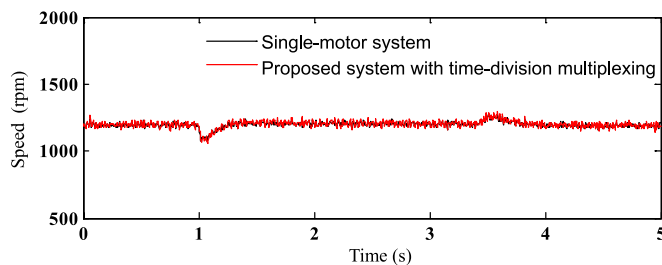


Fig. 11. Experimental results showing a comparison of speed responses between a single-motor system and the proposed four-motor system with time-division multiplexing during step load changes.

motor system and the proposed four-motor system with time-division multiplexing. The experimental results confirm that the proposed system with time-division multiplexing can operate effectively with the same control performance comparing with a single-motor system. Often, the computation time required for one motor is much lower than the switching period of the inverter. This condition implies that several control algorithms can be either allocated in sequential manner as a pipeline operation, or executed in a series of cycles as a time-division multiplexing, as shown in Fig. 12. From the viewpoint of control performance, the proposed four-motor system with time-division multiplexing can permit and extend the operation at higher maximum inverter switching frequency (up to 141 kHz), which is applicable for a high-bandwidth speed and torque control system.

For FPGA resource usage analysis, a comparison of resource utilization on a XCS1600E FPGA for controlling a single-unit and a four-unit PMSM motor drive system is summarized in Table I. It can be seen that due to the limited number of dedicated multipliers available in the FPGA target, it is not possible to fit four identical controller modules into a single device. By considering for four-unit motor system, the proposed solution with time-division multiplexing approach can simplify the entire system into a single hardware module, which improves significantly the total resource utilization. The area performance analysis shows that the total occupied resources for the entire system are perfectly fitted for a single FPGA.

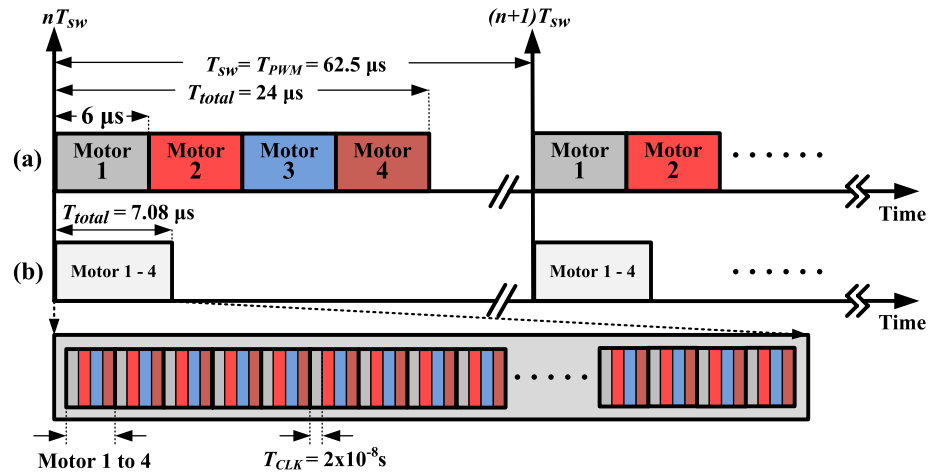


Fig. 12. Comparison of the system-timing diagram for the proposed four-motor control system: (a) Single module with pipelining; (b) Single module with time-division multiplexing.

Table I. Resource utilization for a single-unit and a four-unit PMSM motor drive system

| Unit of motors | Hardware design approach | Occupied Slices (%) | CLB Flip Flops (%) | 4 input LUTs (%) | MULT18X18 ISOs (%) |
|----------------|--------------------------------------|------------------------|--------------------|------------------|--------------------|
| 1 | Single module | 39 | 20 | 34 | 80 |
| 4 | Four identical modules | Insufficient resources | | | |
| | Single module with time multiplexing | 82 | 43 | 77 | 80 |

The overall system consumes 82% of occupied slices, 43% of configurable logic block (CLB) flip flops, 77% of look-up tables (LUTs), and 80% of embedded multipliers of available resources.

5 Conclusions

This paper has presented a fully integrated single chip solution for a cross-coupling multi-motor control system. The proposed single chip solution with a time-division multiplexing scheme allows the entire system to be implemented on a single device. The experimental results confirm that the proposed system can successfully operate a group of four motors simultaneously, allowing the processing data to be internally transmitted among controller modules within the same chip. The proposed solution can be extended to a larger number of motor units, or to other industrial multi-motor control systems, including the recent trend of four-wheel drive electric vehicles.

Appendix

The specifications of the four low-power PMSM motors are given as follows: 100 W, 0.318 Nm, 36 VDC, 4 A, 3000 rpm, 200 Hz, 8 poles, $R_s = 0.3731 \Omega$, $L_d = 1.683 \text{ mH}$, $L_q = 2.041 \text{ mH}$, $\lambda_m = 1.053 \times 10^{-2} \text{ V}\cdot\text{s}$, $J = 1.034 \times 10^{-5} \text{ kg}\cdot\text{m}^2$, $B = 1.349 \times 10^{-6} \text{ Nm}\cdot\text{s}$.